In the outstanding Office Action, the drawings were objected to, and Claims 1-6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Applicant's Figures 15-22 in view of the Japanese patent JP 4-170788.

Before discussing the objection/rejection of the outstanding Office Action, Applicant respectfully requests the IDS filed September 18, 2000, be acknowledged by the Examiner. Further, Applicant notes that the IDS filed on September 18, 2000, contains only one reference and this reference was cited in the outstanding Office Action but not made of record in a Notice of References Cited.

In response to the objection to the drawings, Figures 5, 6, 16, and 18 are being amended to show element sections crosshatched and Figures 15-22 are being labeled "PRIOR ART," as requested in the outstanding Office Action. A separate letter requesting approval of these changes is being submitted to the draftsman. Accordingly, it is respectfully requested that this objection be withdrawn.

Further, the abstract has been amended to remove all references to figures and to correct minor informalities. No new matter has been added.

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Applicant's Figures 15-22 in view of JP 4-170788. This rejection is respectfully traversed.

Amended Claim 1 finds support in the specification at page 11, lines 11-13, and is directed to a multilayered wiring substrate having a plurality of multilayered wiring layers, signal wirings, and dummy wirings. At least one of the multilayered wiring layers has a signal wiring group made of a plurality of signal wirings disposed in parallel to each other. The dummy wirings are disposed in the at least one of the multilayered wiring layers, outside

the signal wiring group and in parallel to the signal wirings of the signal wiring group. At least one of the dummy wirings is disposed at each side of the signal wiring group.

In a non-limiting example, Figure 1 shows the multilayered wiring substrate 100, at least one of the multilayered wiring layers having the signal wirings 31a-31n, and the dummy wirings 31Da and 31Dn. Moreover, the dummy wirings 31Da-31Dn are disposed outside the signal wirings 31a-31n, in parallel with the signal wirings. At least one of the dummy wirings 31Da and 31Dn is disposed at each side of the signal wiring group 31.

By providing the dummy wirings 1) outside the signal wiring group but still inside the layer of the multilayered wiring substrate, and 2) parallel to the signal wirings, a line capacitance of the outermost signal wiring of the signal wiring group can be made equal to a capacitance of other signal wirings.[1] Therefore, a speed of the signals propagating along the signal wirings is identical and a "propagation delay time difference of the signals can be considerably reduced or eliminated."[2] Thus, a memory can be operated more reliable at a high speed because the signals get to the memory without delay.

Applicant's Figures 15-22 show a multilayered wiring substrate having a plurality of multilayered wiring layers, and at least one of the multilayered wiring layers has a signal wiring group made of a plurality of signal wiring disposed parallel to each other. However, Applicant's Figures 15-22 do not teach or suggest dummy wirings disposed in the at least one of the multilayered wiring layers.

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[1]Specification, page 7, lines 6-13.

[2]Id.

JP 4-170788 is asserted in the outstanding Office Action for its teachings of dummy wirings 10A and 10B disposed outside a memory array.[3] JP 4-170788 shows in Figure 1 two adjacent memories 1, a plurality of bit lines 3a and 3b, and "only one" bit line as a dummy bit line pair 10.[4] Further, JP 4-170788 shows in Figure 1 that the dummy bit line pair 10 is disposed completely outside the memory 1. Accordingly, JP 4-170788 does not teach or suggest dummy wirings disposed in at least one of the multilayered wiring layers, outside a signal wiring group, and at least one of the dummy wirings being disposed at each side of a signal wiring group. To the contrary, JP 4-170788 places the dummy lines 10 outside the memory 1. In addition, JP 4-170788 is silent about wirings or specific arrangements of wirings inside the memory 1, or similar shapes for the dummy wirings and the signal wirings inside the memory 1.

Further, JP 4-170788 is related to a technique to prevent voltage differences between two inputs into a sense amplifier from becoming small when a voltage read from a memory cell is amplified by the sense amplifier that performs differential amplification by equalizing capacities of a bit line pair (bit line and $\overline{\text{bit line}}$). In contrast, the device of Claim 1 improves a difference in a delay time between signals propagating along the wirings, which is different both in object and performance from the device in JP 4-170788.

Therefore, it is respectfully submitted that the combination of Applicant's Figures 15-22 and JP 4-170788 does not render obvious Claim 1. Accordingly, it is respectfully submitted that independent Claim 1 and each of the claims depending therefrom are allowable.

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[3]Outstanding Office Action, page 3, second paragraph.

[4]JP 4-170788, abstract.

Moreover, regarding the rejection of Claim 2, Applicant respectfully submits that JP 4-170788 does not teach or suggest any through hole or dummy through hole extending in a stacking direction and conductive layers disposed inside the through holes and dummy through holes, as asserted in the outstanding Office Action at page 3, last paragraph.

Regarding the rejection of dependent Claims 3 and 4, it is respectfully submitted that JP 4-170788 does not teach or suggest a through hole, a dummy through hole, and a conductive layer inside the through hole and dummy through hole, as recited in Claims 3 and 4.

Regarding the rejection of dependant Claim 6, the outstanding Office Action states at page 5, lines 3-5, that Applicant's admitted prior art teaches a terminal 52 "for connecting a terminal resistance." However, the reference number 52 refers to a solder, and thus the above assertion is not accurate. The specification describes at page 3, lines 14-15, that a solder 52 connects a pad of a signal wiring of a signal wiring group 31 and an external lead 51a of a DRAM 51.

In addition, new Claims 7-11 have been added to set forth the invention in a varying scope and Applicant submits the new claims are supported by the originally filed specification. In particular, new Claim 7 recites that a distance between a dummy wiring adjacent to a signal wiring and the respective signal wiring is the same as a distance between any adjacent two signal wirings. Claims 8 and 9 are identical but depend on Claims 1 and 7, respectively. Claims 7 and 8 recite that any distance between two adjacent wirings from the signal wirings and the dummy wirings is the same. New independent Claim 10 includes the subject matter of Claims 1 and 2, and new Claim 11 is identical to Claim 3 but depends on

new Claim 10. Therefore, it is respectfully submitted that new Claims 7-11 are allowable for similar reasons as discussed above.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to this effect is respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

Please amend Claim 1 as follows:

--1. (Amended) A multilayered wiring substrate, comprising:

a plurality of multilayered wiring layers, at least one of said multilayered wiring layers [containing] comprising a signal wiring group made by a plurality of signal wirings disposed in parallel with one another; and

dummy wirings disposed in said at least one of said multilayered wiring layers, outside said signal wiring group, and in parallel to said signal wirings, at least one of said dummy wirings being disposed at each side of said signal wiring group.--

Claims 7-11. (New).

IN THE ABSTRACT

Page 23, lines 1-15, please amend the abstract to read as follows:

[ABSTRACT OF THE DISCLOSURE]

ABSTRACT

Each wiring layer of a multilayered wiring substrate [(100) comprises] includes signal wirings [(3la to 31n] disposed in parallel with one another, and dummy wirings [(31Da, 31Dn)] disposed at each side parallel to the signal wirings of the signal wiring group [(31)] made by signal wiring [(31b to 31m)], respectively. The dummy wirings [31Da, 31Dn)] have the same shape as the signal wirings [(31a to 31n)], and are disposed in parallel to the signal wirings [(31b to 31m)] at the same intervals as that in the signal wirings [(31a to 31n)]. Through holes [(40ab to 40mn)] are formed in the respective clearances among the signal wirings [(3la to 31n)]. Dummy through holes [(40Da, 40Dn)] having the same shape as the through holes [(40ab to 40mn)] are formed between the dummy wiring [(31Da, 31Dn)] and signal wiring [(31a, 31n)]. A conductive layer is formed on the inner wall of the through holes [(40ab to 40mn, 40Da, 40Dn)]. [With the] The multilayered wiring substrate [(100), it] is able to reduce or eliminate the delay time difference between signals that propagate along the signal wirings.